Stress and Characterization Strategies to Assess Oxide Breakdown in High-Voltage GaN Field-Effect Transistors

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Outline

- Motivation & Challenges
- Time-Dependent Dielectric Breakdown (TDDB) Experiments:
  - Current-Voltage
  - Capacitance-Voltage
- Conclusions

Motivation

- GaN Field-Effect Transistors (FETs) promising for high-voltage power applications
- Many challenges before transistors ready for deployment:

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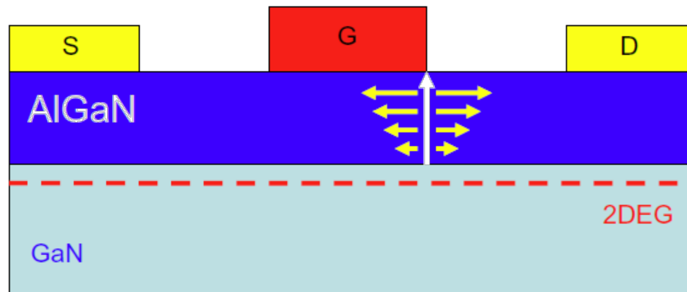

Inverse piezoelectric effect
J. A. del Alamo, MR 2009

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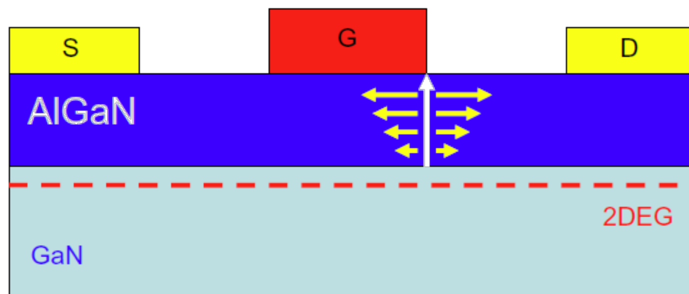

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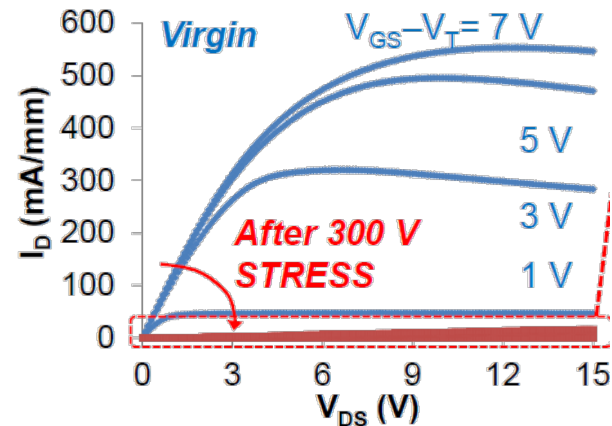

Current collapse

D. Jin, IEDM 2013

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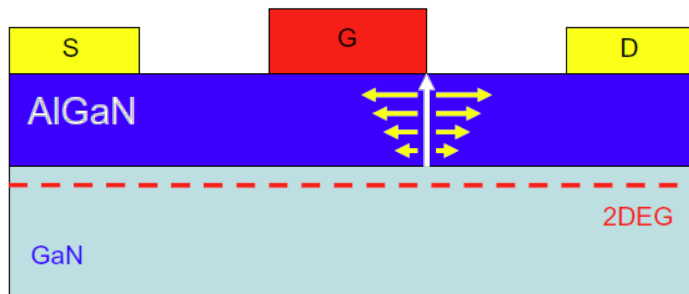

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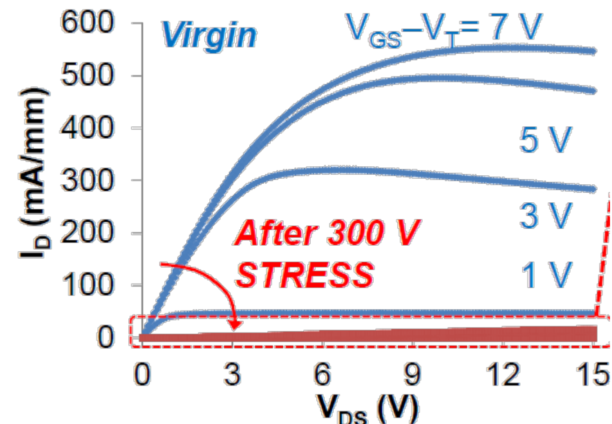

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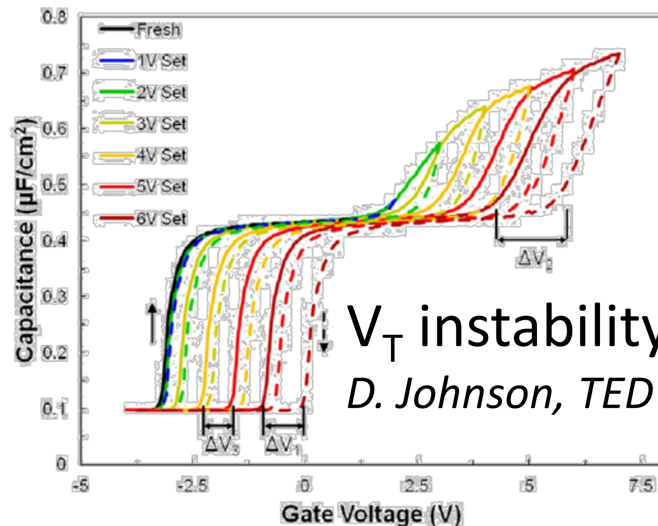

V_T instability

D. Johnson, TED 2013

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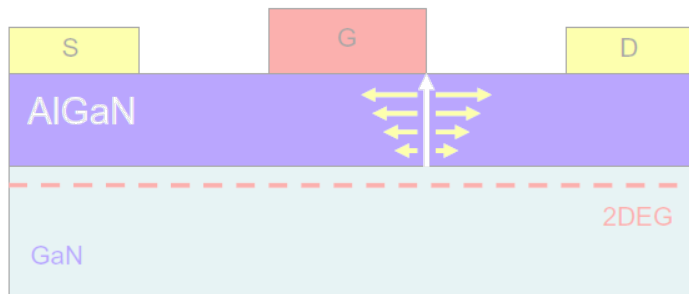

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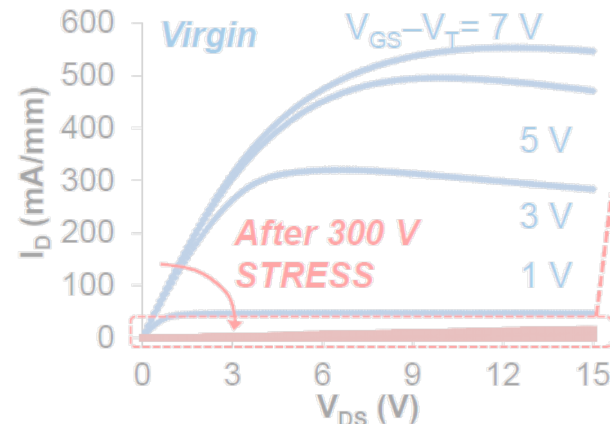

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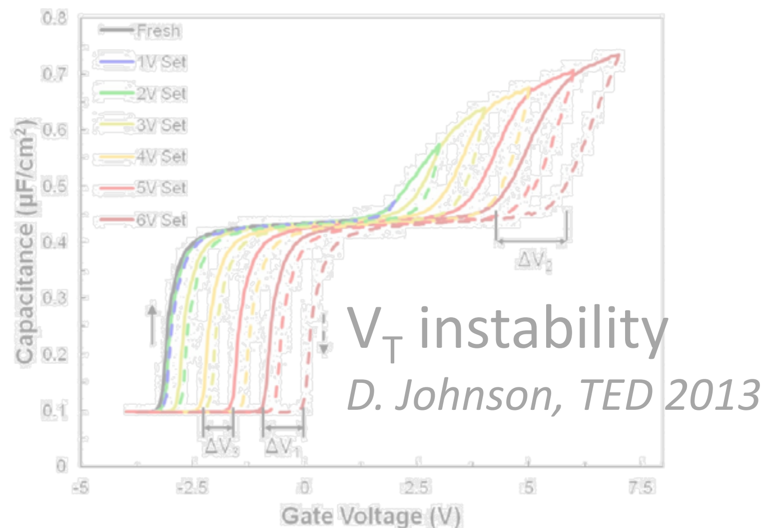


V_T instability

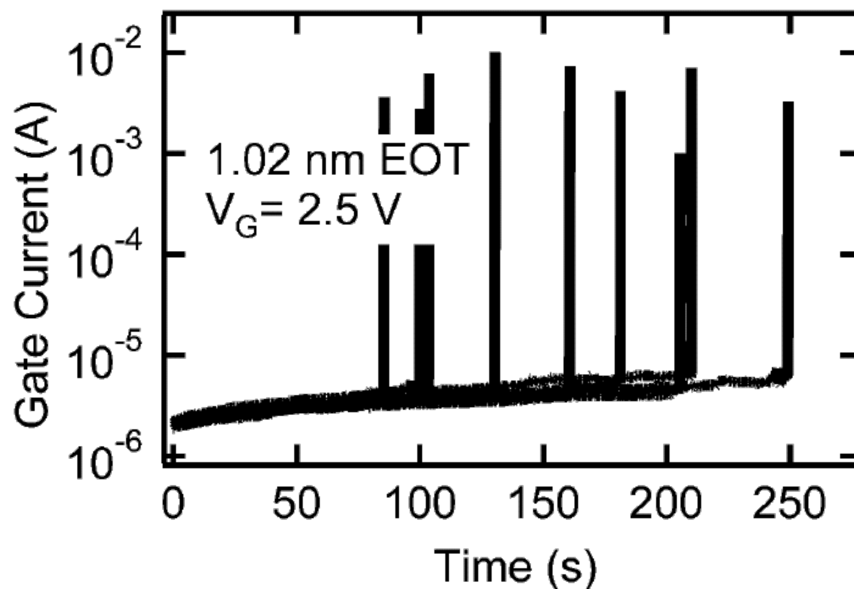
D. Johnson, TED 2013

Oxide reliability

Time-Dependent Dielectric Breakdown

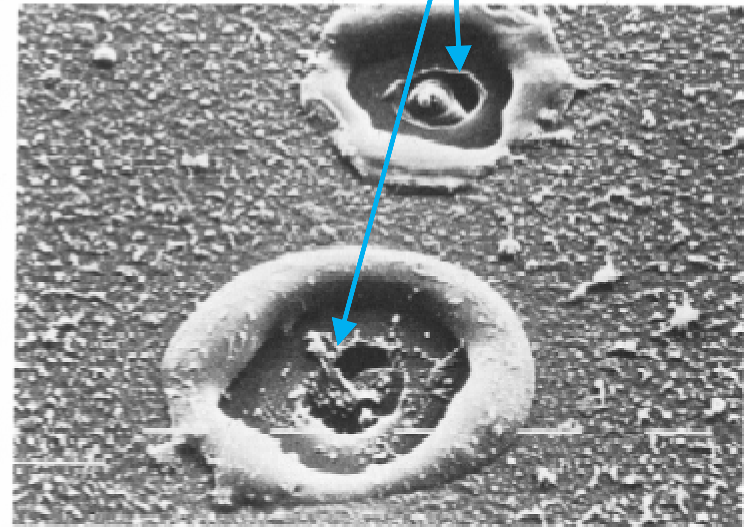
- High gate bias → defect generation → catastrophic oxide breakdown
- Often dictates lifetime of chip

Typical TDDB experiments:
Si high-k MOSFETs



T. Kauerauf, EDL 2005

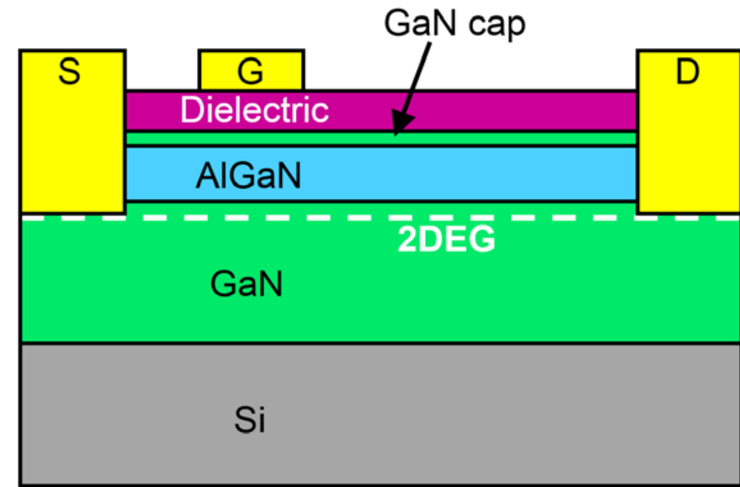
Gate material melted after breakdown



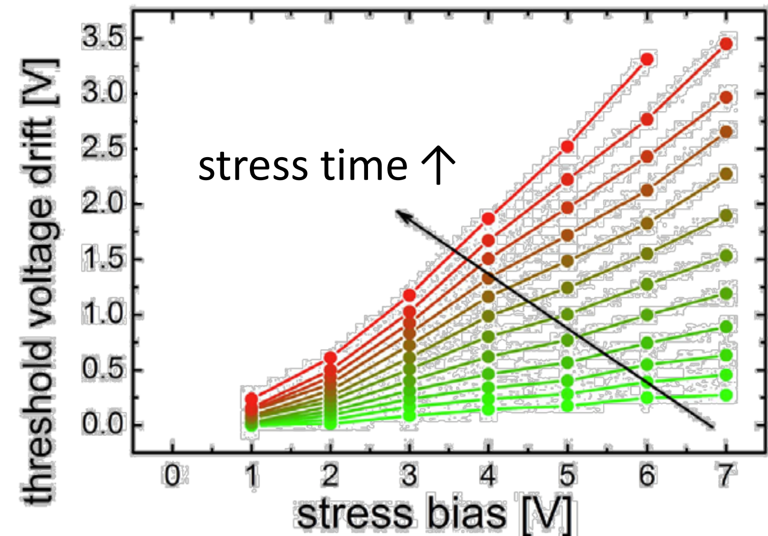
D. R. Wolters, Philips J. Res. 1985

Challenges to study TDDB in GaN FETs

- AlGaN/GaN metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs)



- Gate stack has multiple layers & interfaces
  - → Uncertain electric field distribution
  - → Many trapping sites
- Complex dynamics involved
  - → Unstable and fast changing V_T

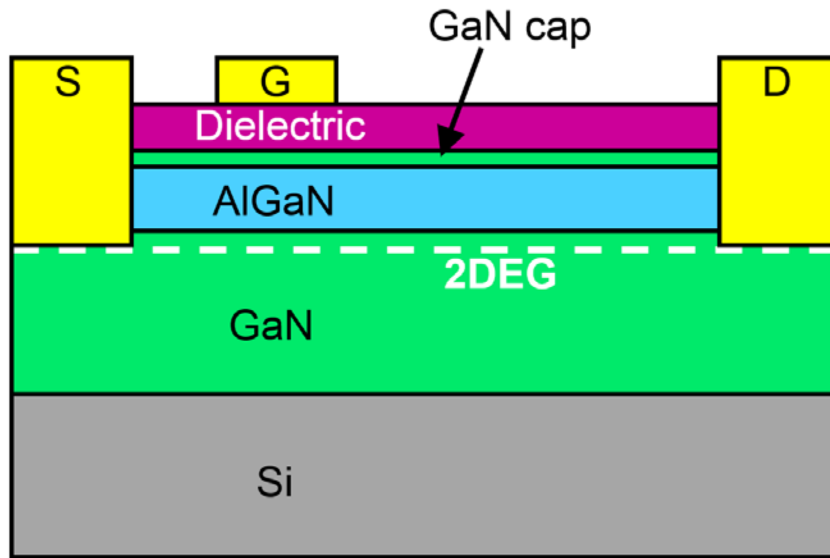


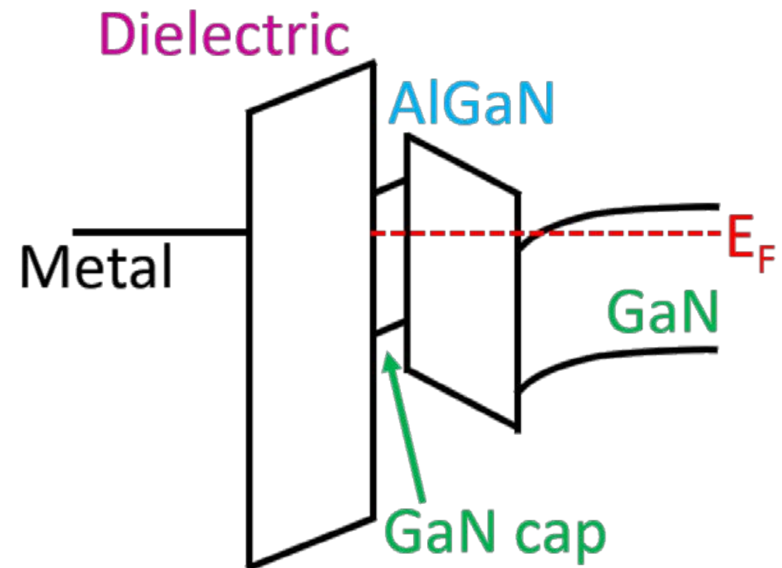
P. Lagger, TED 2014

TDDB Experiments: Current-Voltage

GaN MIS-HEMTs for TDDB study

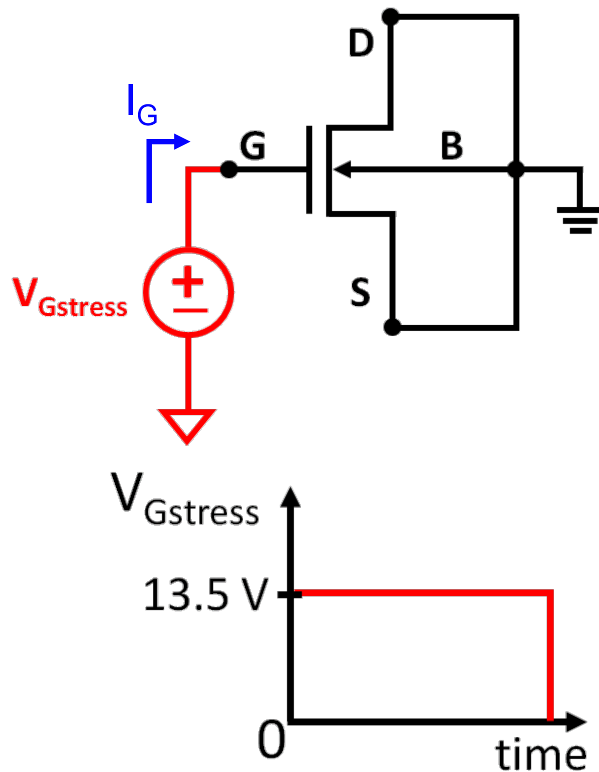
GaN MIS-HEMTs from industry collaboration: depletion-mode

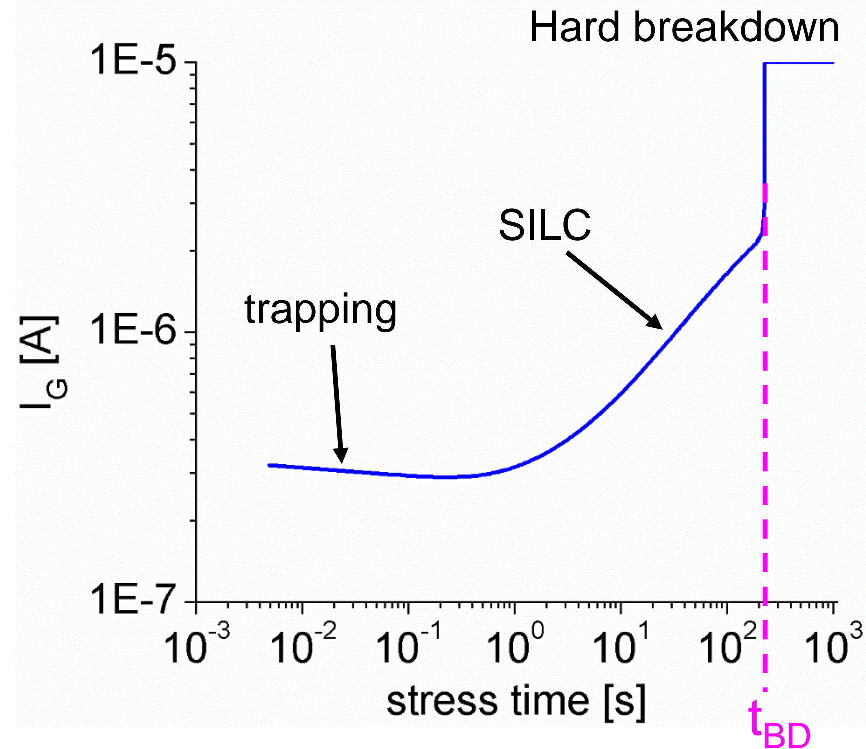




Classic TDDB Experiment

Constant gate voltage stress experiment:

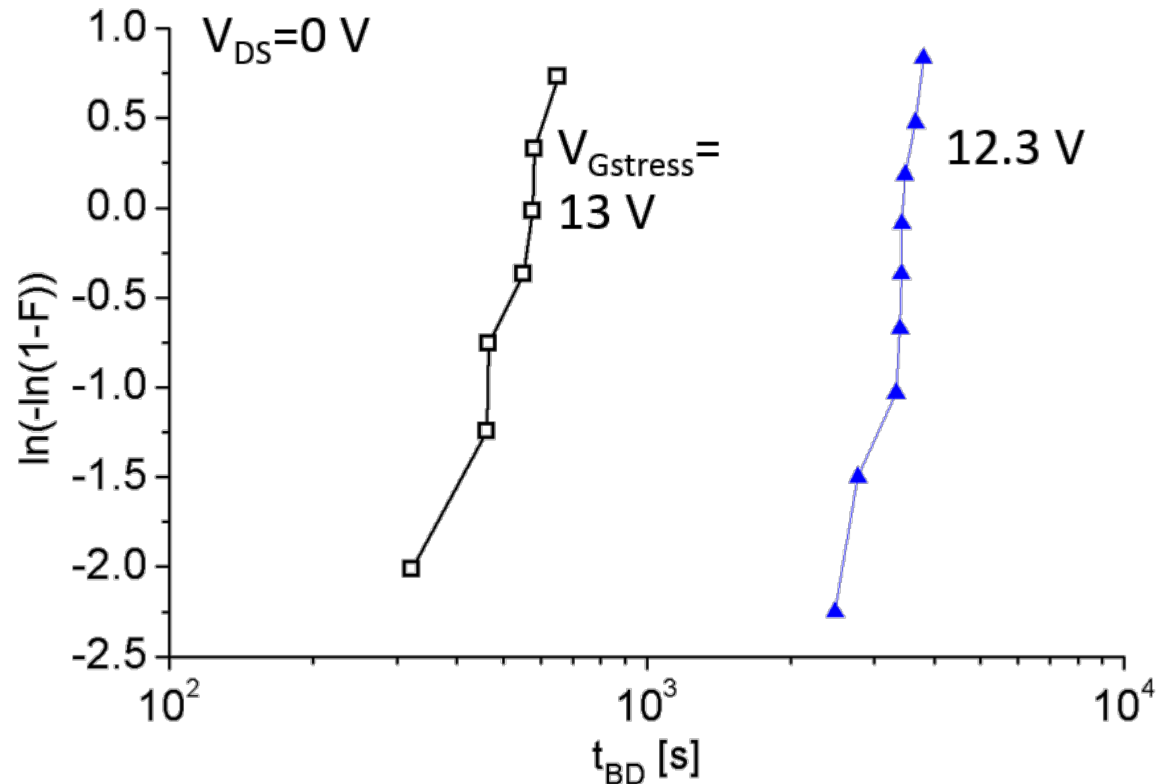




- Experiment gives time to breakdown and shows generation of *stress-induced leakage current* (SILC)
- Little other insight gained from measurement

Visualizing TDDB Statistics

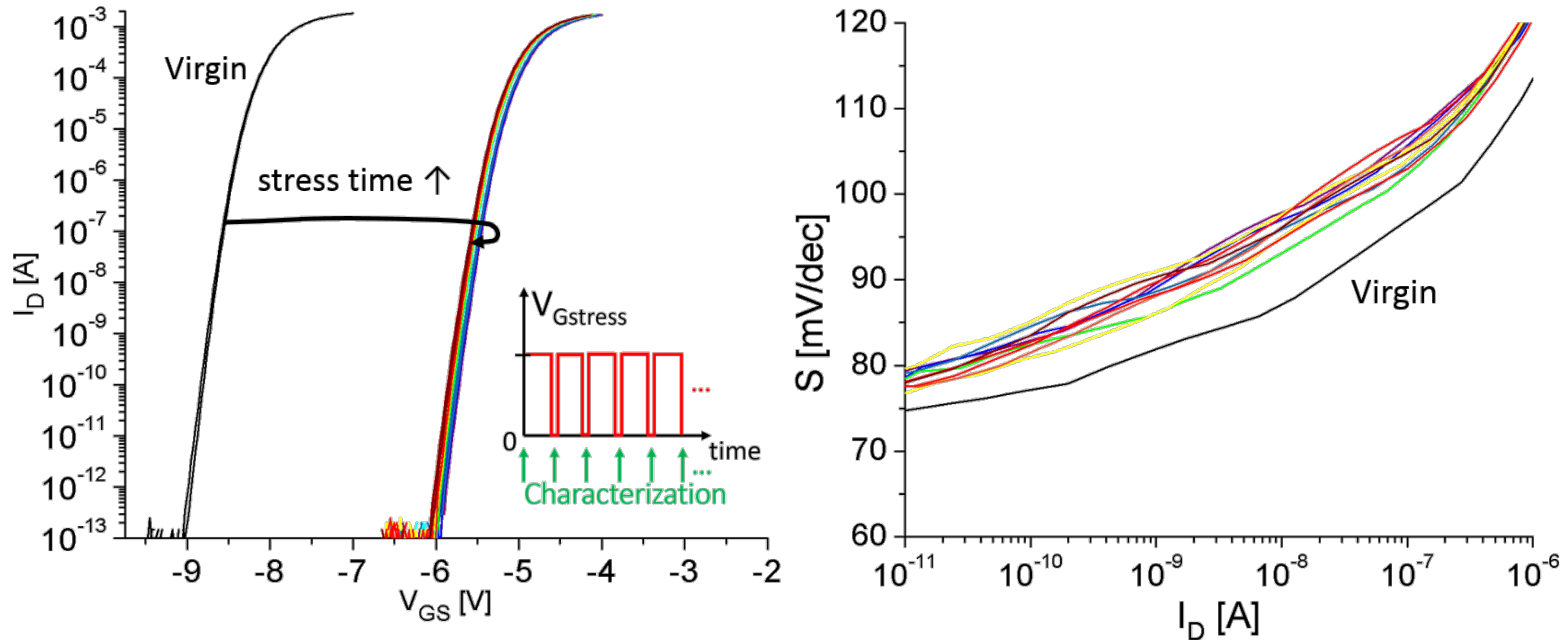
TDDB uniqueness: Weibull distribution of time to breakdown



- As $V_{Gstress}$ ↑, t_{BD} ↓
- Parallel distributions for different $V_{Gstress}$

TDDB with Periodic Characterization

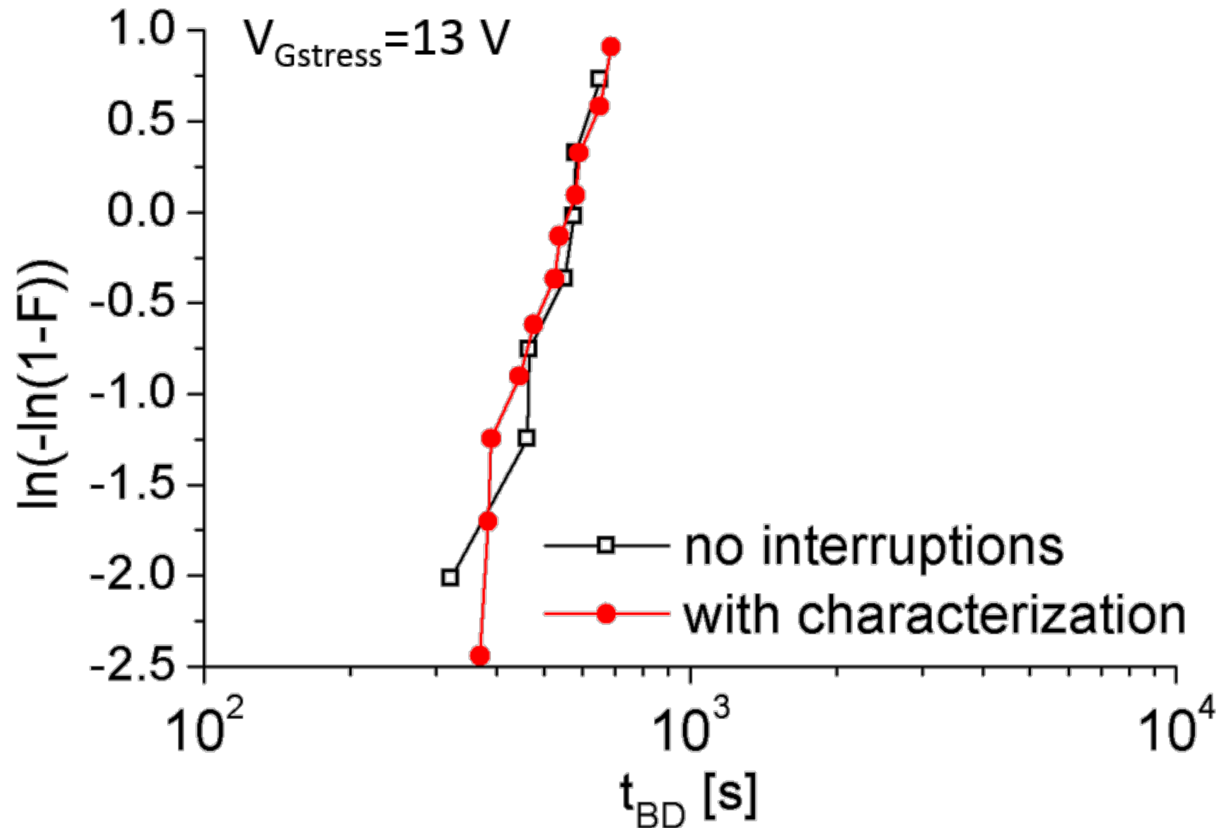
Pause TDDB stress and sweep transfer characteristics at V_{DS}=0.1 V



- Large V_T shift → trapping in oxide or AlGaN
- Immediate S degradation → interface state generation early in experiment

Validity of Characterization Approach

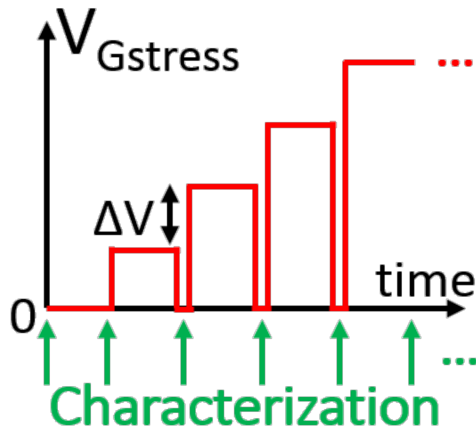
Compare statistics for standard and interrupted schemes

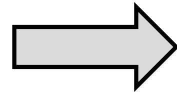


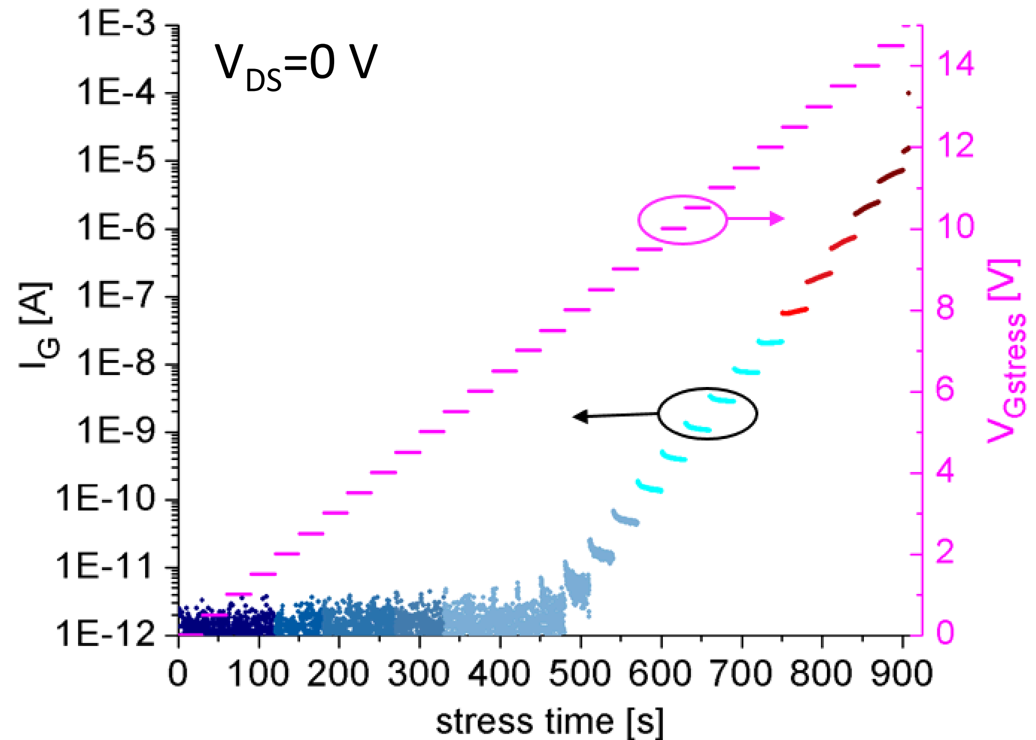
Same statistics for both schemes → characterization is benign

Step-Stress TDDB

- Step-stress to examine early stages of degradation
- Step $V_{Gstress}$ in 0.5 V increments until breakdown



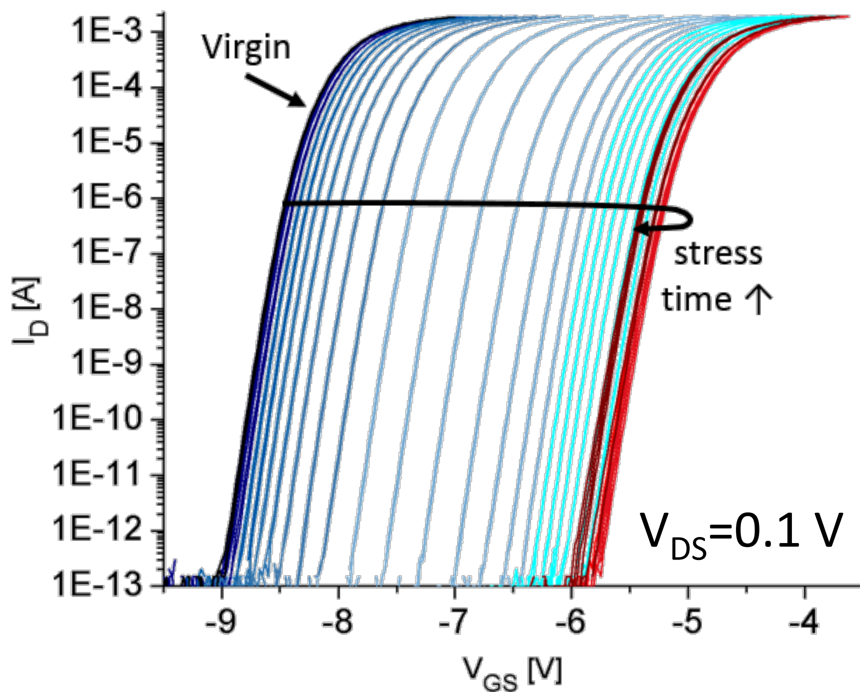


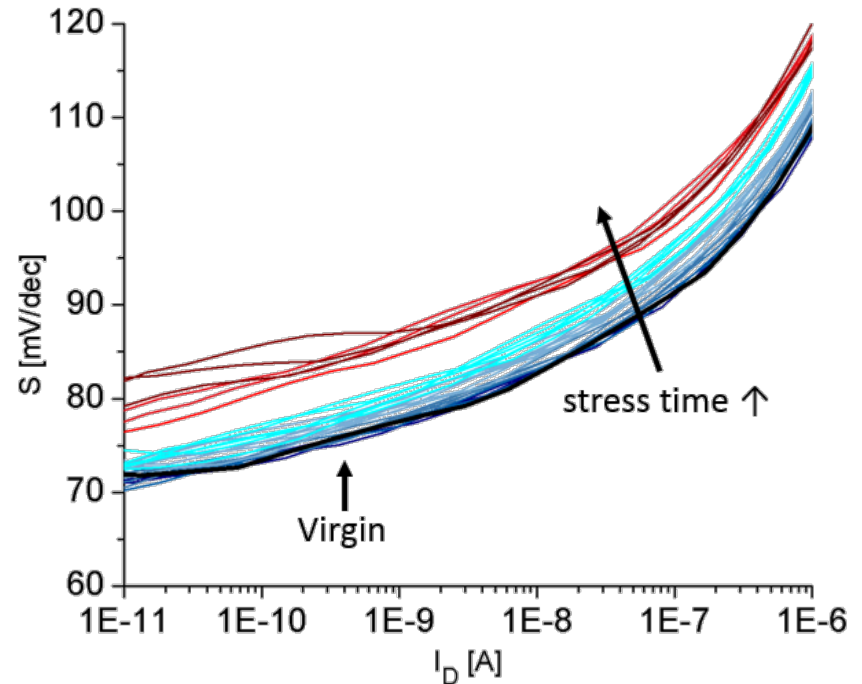


- Low $V_{Gstress}$: $I_G \downarrow \Rightarrow$ trapping
- High $V_{Gstress}$: $I_G \uparrow \Rightarrow$ SILC

Step-Stress TDDB

Transfer characteristics during Step-Stress TDDB

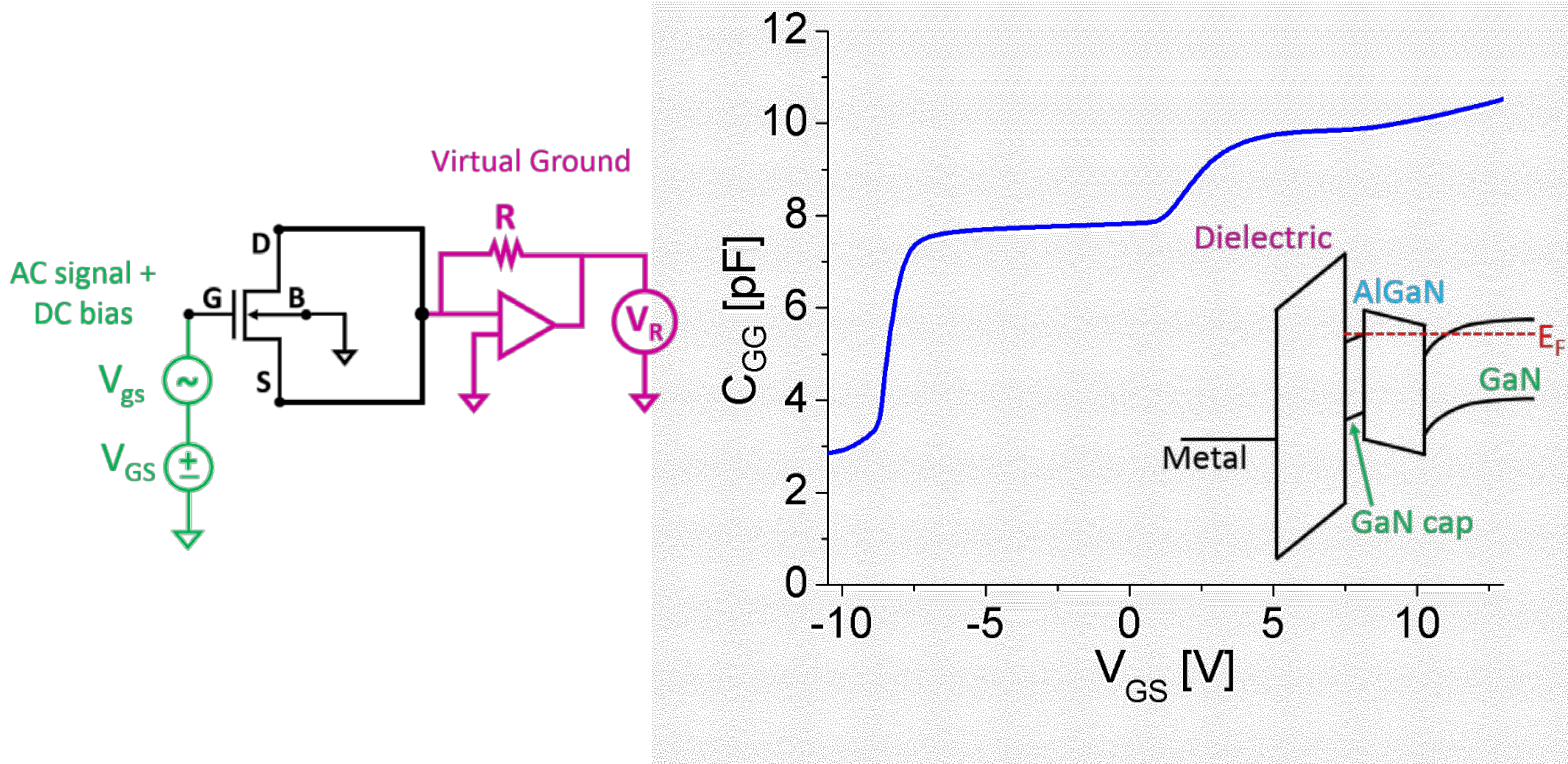




- S and V_T degradation is progressive
- At $V_{Gstress}$ ~12.5 V, ΔV_T < 0 (red lines)
  - Sudden increase in S, appearance of SILC→ interface state generation

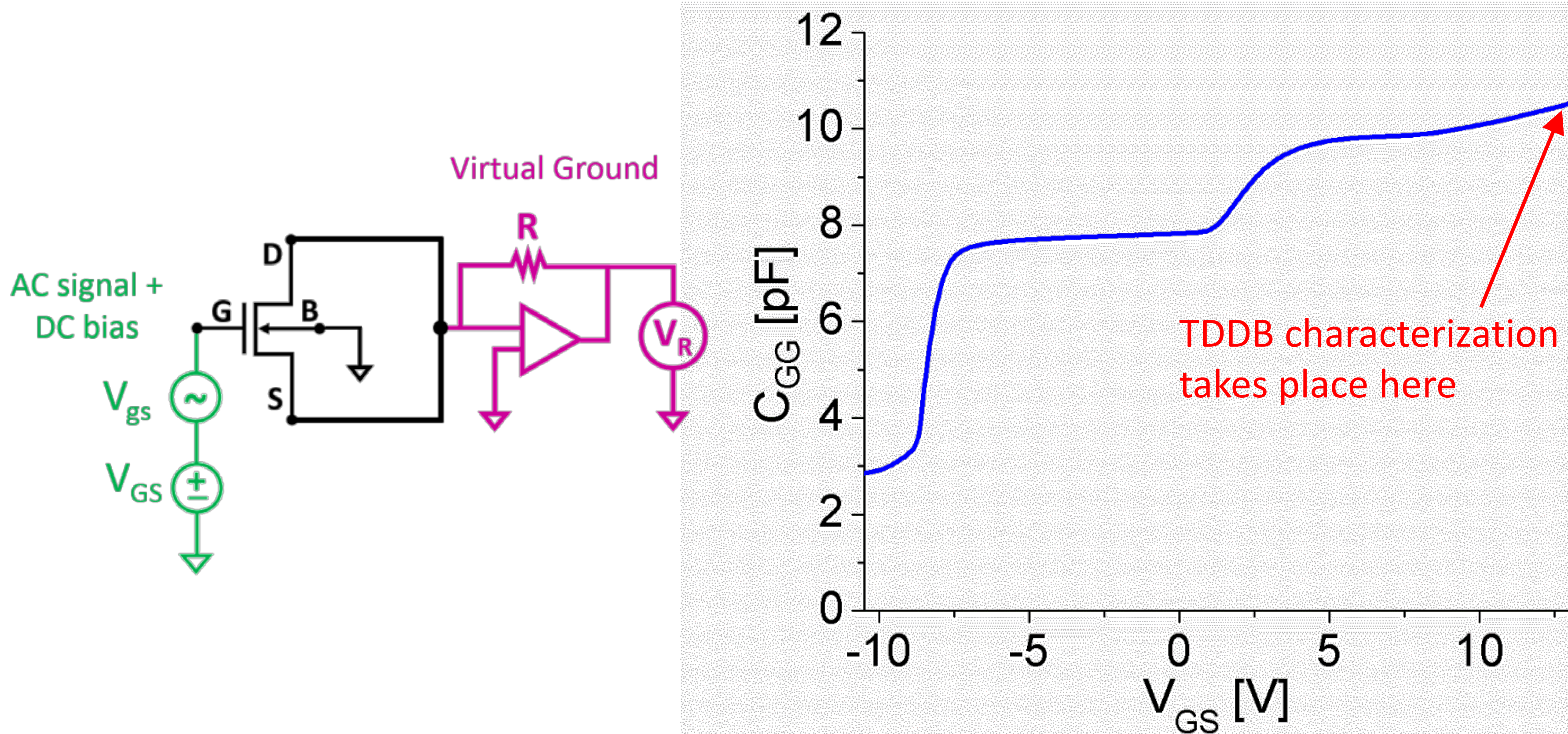
TDDB Experiments: Capacitance-Voltage

C-V Characterization



- At V_{GS}>1 V, conduction band of GaN cap starts being populated

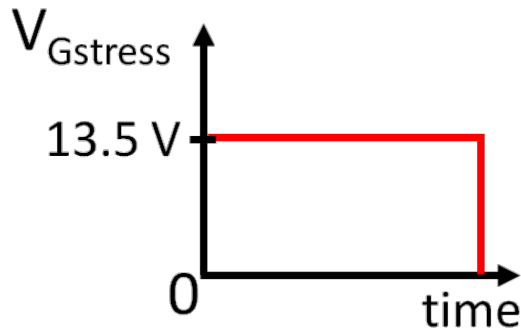
C-V Characterization

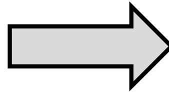


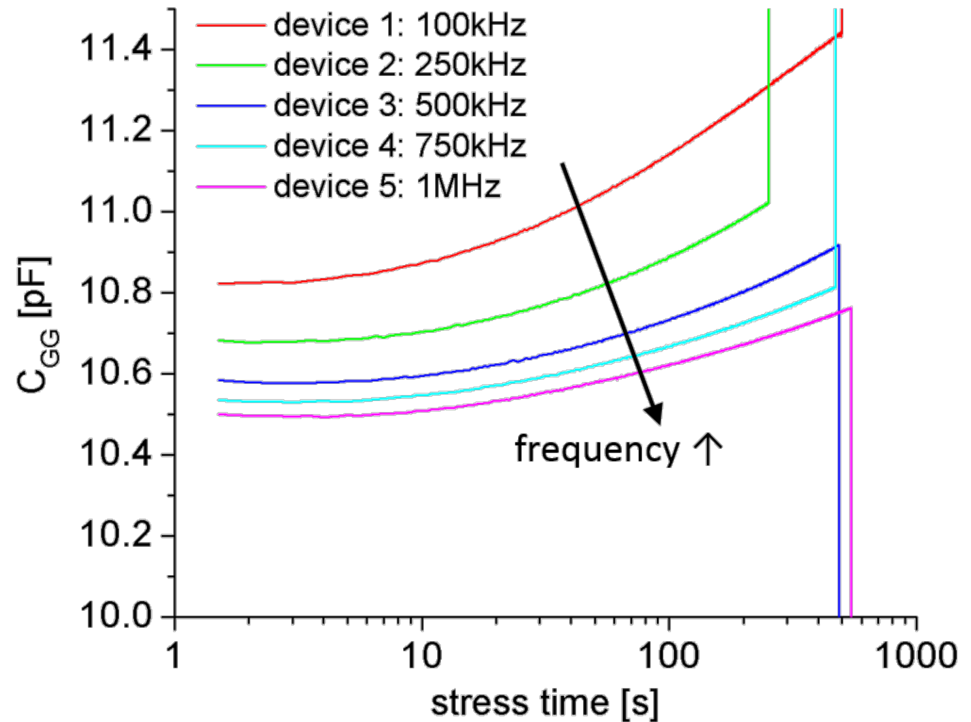
- TDDB characterized in regime where GaN cap is populated with electrons

Constant $V_{Gstress}$ TDDB

C_{GG} vs. stress time in 5 devices at 5 different frequencies:

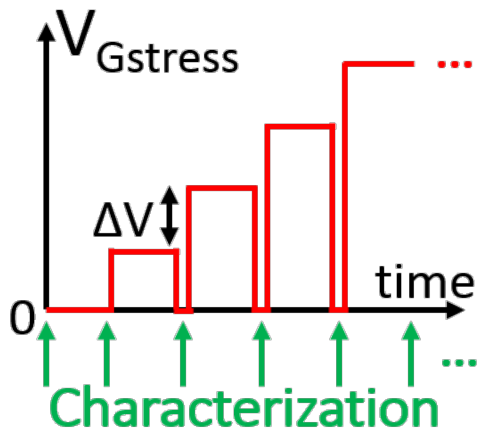


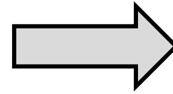


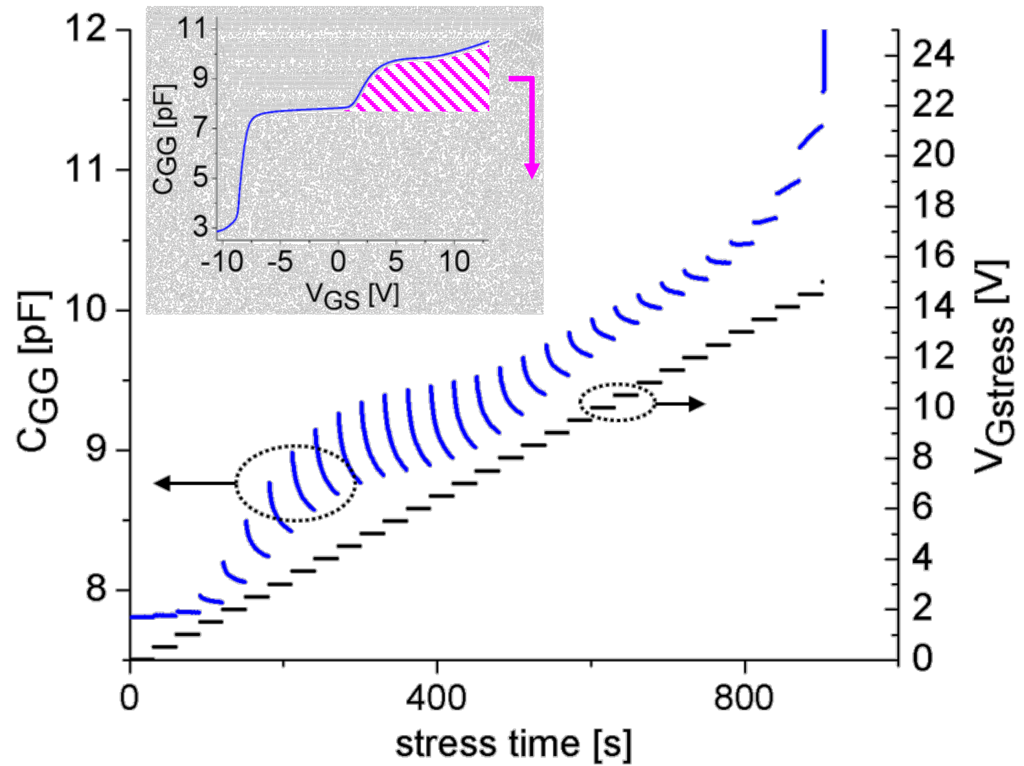


- As stress time ↑
  - → C_{GG} ↑
  - → Frequency dispersion ↑
- Consistent with trap creation and trapping
  - In oxide and/or at MOS interface

Step-Stress TDDB

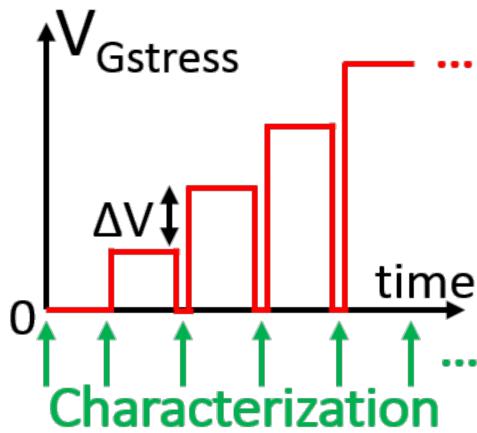


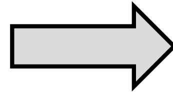


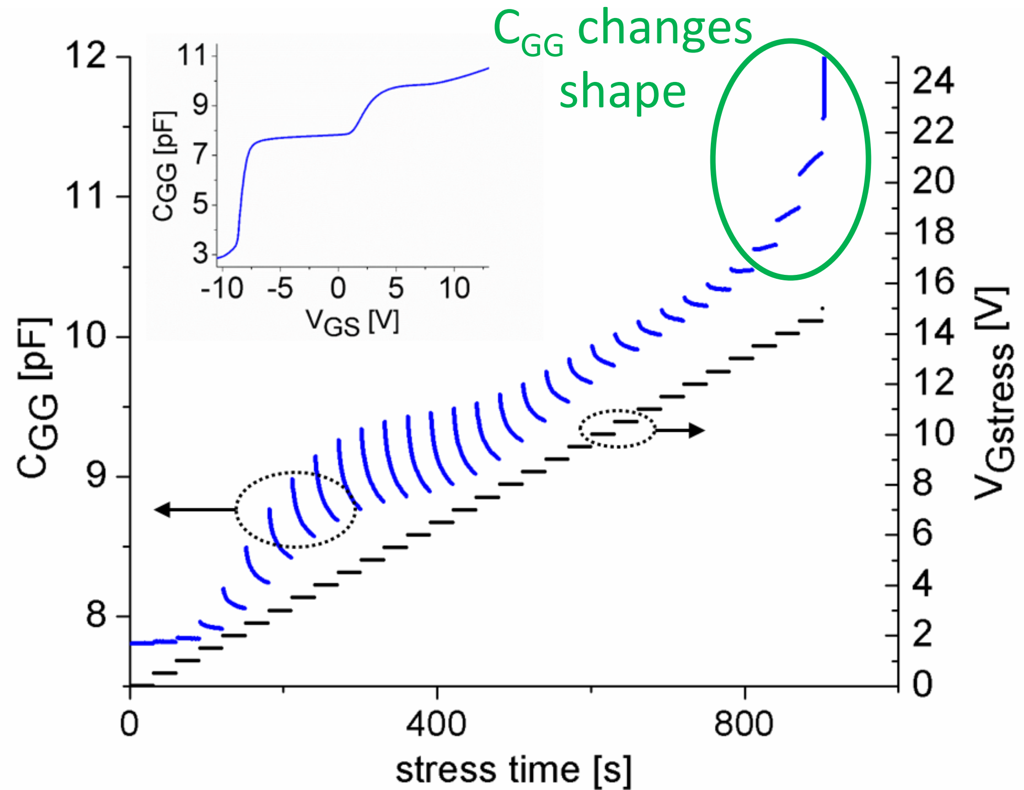


- Moderate $V_{Gstress} \rightarrow C_{GG} \downarrow \Rightarrow$ trapping in AlGaN

Step-Stress TDDB







- Moderate $V_{Gstress}$ → C_{GG} ↓ ⇒ trapping in AlGaN
- High $V_{Gstress}$ → C_{GG} ↑ ⇒ trap generation in oxide

Conclusions

- Developed methodology to study TDDB in GaN MIS-HEMTs
- TDDB behavior consistent with Si MOSFETs:
  - Weibull distribution
  - SILC before breakdown
- For moderate gate voltage stress:
  - $\Delta V_T > 0$
  - $I_G \downarrow$
- Beyond critical value of $V_{Gstress}$:
  - $\Delta V_T < 0$
  - Sudden $\Delta S \uparrow$
  - Capacitance frequency dispersion $\uparrow$

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  Onset of trap generation in oxide/at MOS interface

Acknowledgements

Questions?